REMARKS

This is intended as a full and complete response to the Office Action dated December 22, 2004 (hereinafter "the Office Action") having a shortened statutory period for response set to expire on March 22, 2005.

Claim 16 was amended to add the word span to the describing element to more expressly recite that which was claimed in that claim prior to the amendment. Claims 1- 20 remain in the above-captioned application.

Claims 1-20 were rejected under 35 U.S.C. §102(a/e) as being anticipated by U.S. Patent No. 6,349,403 B1 ("Dutta"). With this rejection, applicant respectfully disagrees, at least for the reasons set forth below.

Dutta asserts in Figure 1 and Column 2, lines 26-58 potential problems with grid-based routers on an integrated with several different custom circuit designs. Thus Dutta discloses a router where "...a grid array of predefined equally spaced horizontal and vertical lines is not used for routing wire connections between the source and the target." [column 6, lines 27-30]. Rather, Dutta discloses that "escape lanes are used for routing wire connections and the lanes are based on the boundaries (e.g., the edges) of obstructions within the layout." [column 6, lines 31-33], where "... obstructions (e.g., circuit blocks, etc.) 262, 264, 266 and 268 ... do not allow the routing of wire connections there within." [column 8, lines 26-29]. Figures 7 and 8 show routing show examples of routes from source (S) to target (T) using these escape lanes. In addition Dutta discloses in Figure 8, column 13, lines 7-25, that circuit blocks, e.g., 486 and 488, can be ignored because they are on a different layer than the lane 504.

In contrast amended claim 1 comprises determining a respective span in terms of one or more of the topology units for each of the routing resources, wherein each of the topology units are same or similar to the other topology units. This is supported by Figure 7 and paragraphs [0048] to [0051] of the specification, where in one embodiment the topological units are tiles in an FPGA. Each tile is a region of logic and routing resources, which is replicated throughout the FPGA. Hence claim 1 is more like grid based routing than gridless routing as in Dutta. Therefore Dutta not only

does not disclose the above feature of claim 1, but teaches away from it. For this reason alone claim 1 should be allowable.

For at least the reasons given for claim 1 each of the independent claims 8, 12, 13, 14, 15, and 16, are not described, shown, or suggested by Dutta, and thus each of such claims is allowable. Furthermore, it is respectfully submitted that claims 2-7, 9-11, and 17-20, which depend either directly or indirectly upon an allowable base claim, are likewise allowable.

Claims 4, 7, 11, and 19-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dutta. With this rejection, applicant respectfully disagrees, at least for the reasons set forth below.

As mentioned above, Dutta employs a gridless approach. A gridless approach as in Dutta does not describe, show, or suggest span in terms of topology units as discussed above. In contrast to Dutta, claim 4 recites in relevant part that the topology units are associated with programmable logic blocks. Dutta does not define span in terms of topology units and does not disclose programmable logic blocks. Accordingly, it is respectfully submitted that claim 4 is patentable in plain view of Dutta. Moreover, it is respectfully submitted that claim 4, as being dependent upon an allowable base claim, is likewise allowable for the reasons set forth above with respect to the rejection of claim 1.

With respect to claims 7 and 11, Dutta does not describe, show, or suggest identification of a number of topology units with which a routing resource intersects as claimed in those claims. Dutta does not define span in terms of topology units, as previously mentioned. Accordingly, it is respectfully submitted that claims 7 and 11 are patentable in plain view of Dutta. Moreover, it is respectfully submitted that claims 7 and 11, each of which depend upon a respective allowable base claim, are likewise allowable for the reasons set forth above with respect to the rejection of claim 1 and 8.

It is respectfully submitted that claims 19 and 20, which depend upon an allowable base claim, are likewise allowable for the reasons set forth above with respect to the rejection of claim 16.

Applicant brings to the attention of the examiner that Page 2 of the Substitute for Form 1449A/PTO filed with the Information Disclosure Statement on April 5, 2004

for this application was not returned initialed with the First Office Action. Applicant encloses a copy of Page 2 for the convenience of the examiner and requests a copy be returned initialed with the next action.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 16, 2005.

Pat Slaback
Name

Pat Slaback
Signature

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application / Conf. No.	10/600,846 / 8489
Filing Date	June 19, 2003
First Named Inventor	Raymond Kong
Art Unit	2818
Examiner Name	Unknown
Attorney Docket Number	X-1317 US

OTHER – NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		J. Soukup; "Fast Maze Router"; Proceedings of Design Automation Conference, 1978; pp. 100-102.	
		Bryan T. Preas et al.; "Physical Design Automation of VLSI Systems"; The Benjamin/Cummings Publishing Company, Inc.; Copyright 1988; pp. 163-167.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.